ADM-XRC-9R1B
User Manual

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1 Introduction

The **ADM-XRC-9R1B** is a high-performance 8 channel 6GSPS ADC and 8 channel 10GSPS DAC RF XMC for applications using Zynq Ultrascale+ RFSoC from Xilinx.

Figure 1 : ADM-XRC-9R1-B

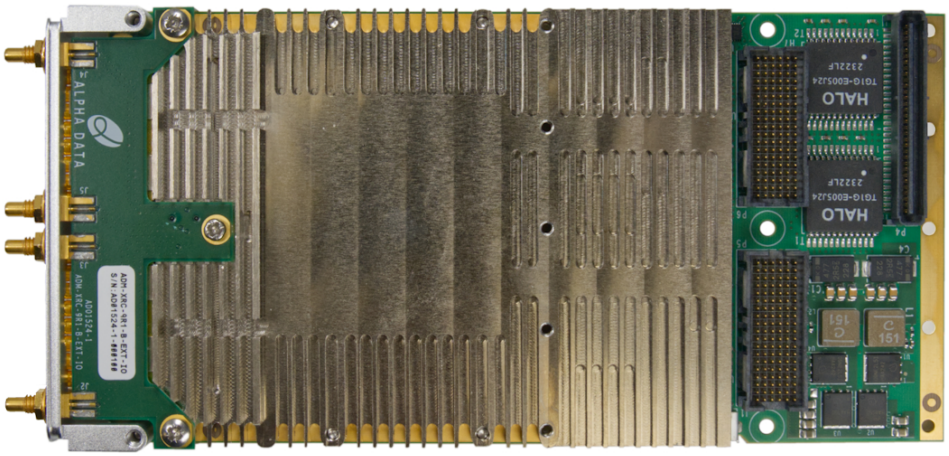

Figure 2 : ADM-XRC-9R1-B

1.1 Key Features

Key Features

- Single-width XMC, compliant to VITA Standard 42.0, 42.3 and 42.10d12
- Support for Zynq Ultrascale+ XCZU47DR/XCZU48DR/XQZU48DR RFSoC in FFVE1156 packages
- Processing System (PS) Block consisting of:
  - Quad-core ARM Cortex-A53, Dual-core ARM Cortex-R5, Mali-400 GPU
  - 1 bank of DDR4-2400 SDRAM 2GB
  - Removable microSD Flash memory
  - Two Quad SPI Flash memory, 512Mb each
  - Two USB ports to rear P4 connector
  - Two serial COM port interfaces to rear P4 connector
  - One system monitor USB port to micro USB connector
  - Two Gigabit Ethernet interfaces to rear P4 connector
  - 4 lane PCI-Express Gen 2 interface on the P5 connector
- Programmable Logic (PL) block consisting of:
  - 8 HSSIO links to the P6 connector
  - 2 banks of DDR4-2400 SDRAM, 1GB per bank
  - 19 GPIO pins
- RF Sampling block consisting of:
  - 8 12/14-bit 4/5GSPS RF-ADCs (Gen1/Gen3)
  - 8 14-bit 6.5/10GSPS RF-DACs (Gen1/Gen3)
  - 8 soft-decision FECs (ZU48DR only)
  - 10MHz to 6GHz -3dB Bandwidth
  - Full Scale Input (100MHz): TBD dBm
  - Full Scale Output (100MHz/20mA Mode): -2.0 dBm
  - Full Scale Output (100MHz/32mA Mode): TBD dBm
- Front Panel IO Interface with:
  - 8 HF single ended ADC signals
  - 8 HF single ended DAC signals
  - Reference clock input for the RF sampling blocks
  - Reference clock output from RF sampling blocks
  - 2 digital GPIO
- Voltage and temperature monitoring
- Board management via USB.
- Air-cooled and conduction-cooled configurations
- Board weight (without cooling metalwork): 101g

1.2 Order Code

ADM-XRC-9R1-B/z-y(c)(a)(x)/(l)

Name	Symbol	Configurations
Device	z	ZU47, ZU48, XQZU48
Speed Grade	y	1, 2
Cooling	c	/AC1 = air cooled industrial /CC1 = conduction cooled industrial
Coating	c	Blank = No Coating /A = Acrylic /P = Polyurethane
XMC Connector	x	Blank = Vita 42 /X2 = Vita 61 XMC2 /V88 = Vita88 XMC+
Lead	l	Blank = Lead-free /PB = Lead build

Table 1 : Build Options

Not all combinations are available. Please check with Alpha Data sales for details.

1.3 References & Specifications

ANSI/VITA 42.0	*XMC Standard*, December 2008, VITA, ISBN 1-885731-49-3
ANSI/VITA 42.2	*XMC Serial RapidIO Protocol Layer Standard*, Feb 2006, VITA, ISBN 1-885731-41-8
ANSI/VITA 42.3	*XMC PCI Express Protocol Layer Standard*, June 2006, VITA, ISBN 1-885731-43-4
ANSI/VITA 46.9	*PMC/XMC Rear I/O Fabric Signal Mapping on 3U and 6U VPX Modules Standard*, November 2010, VITA, ISBN 1-885731-63-9
ANSI/IEEE 1386-2001	*IEEE Standard for a Common Mezzanine Card (CMC) Family*, October 2001, IEEE, ISBN 0-7381-2829-5
ANSI/IEEE 1386.1-2001	*IEEE Standard Physical and Environmental Layers for PCI Mezzanine Cards (PMC)*, October 2001, IEEE, ISBN 0-7381-2831-7
ANSI/VITA 20-2001 (R2005)	*Conduction Cooled PMC*, February 2005, VITA, ISBN 1-885731-26-4

Table 2 : References

2 RF Performance

2.1 Gen3 ADC Performance

Measurement	Conditions/Comments	Value	Unit
Resolution		14	Bits
Sample Rate		1.0-5.0	GS/s
Full Scale Input	Voltage into RF connector (50R) @100MHz	1.20	Vpk-pk
Full Scale Input	Power into RF connector (50R) @100MHz	5.5	dBm
ADC Insertion Loss			
Lower bandwidth	-3dB insertion loss	2.5	MHz
Upper bandwidth	-3dB insertion loss	6.0	GHz
Lower bandwidth	-2dB insertion loss	3.0	MHz
Upper bandwidth	-2dB insertion loss	5.2	GHz
Lower bandwidth	-1dB insertion loss	4.0	MHz
Upper bandwidth	-1dB insertion loss	3.5	GHz
ADC Return Loss			
Lower bandwidth	-10dB return loss	8.0	MHz
Upper bandwidth	-10dB return loss	6.0	GHz
Crosstalk			
Crosstalk	Power received with 0dBm into aggressor channel, 0-6GHz	-55	dBm
Crosstalk	Power received with 0dBm into aggressor channel, 0-3GHz	-65	dBm

Table 3 : ADC Parameters

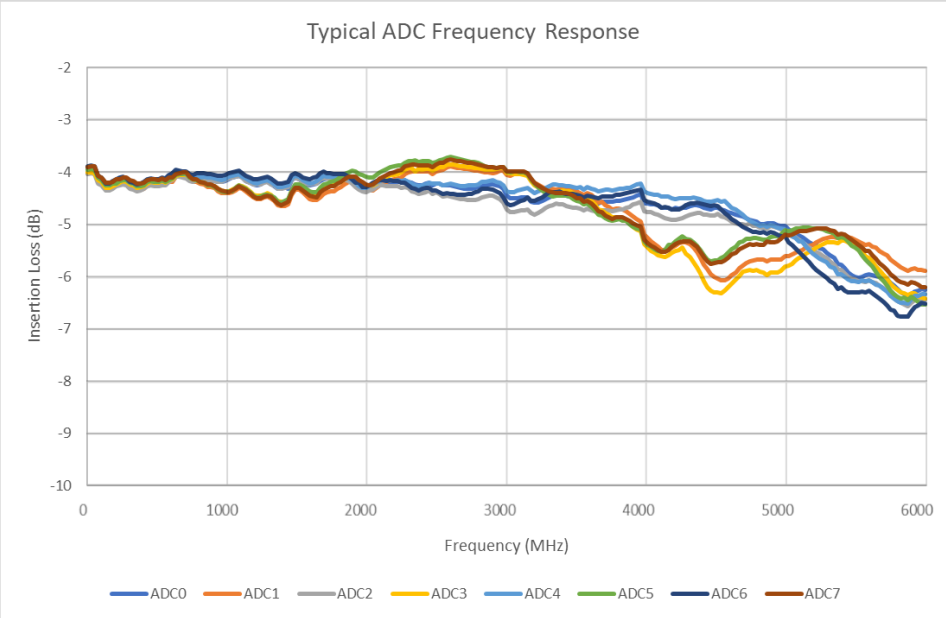

Figure 3 : ADM-XRC-9R1B Gen3 RFSoC ADC Frequency Response

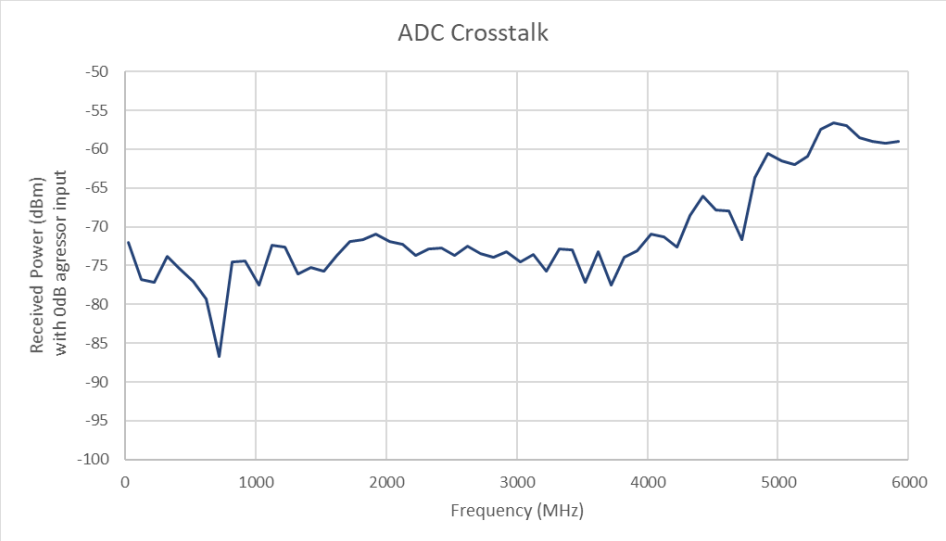

Figure 4 : ADM-XRC-9R1B Gen3 RFSoC ADC Crosstalk

2.2 Gen3 DAC Performance

Measurement	Conditions/Comments	Value	Unit
Resolution	-	14	Bits
Sample Rate	-	0.5 - 10.0[1]	GS/s
Crosstalk	0-6GHz	-45	dBm
Crosstalk	0-3GHz	-52	dBm
Full Scale Output	Voltage out of RF connector, 40.5mA, 50R termination	1.0	Vpk-pk
Full Scale Output	Power out of RF connector, 40.5mA, 50R termination	3.9	dBm

Table 4 : DAC Parameters

[1]: Maximum sample rate depends on speed grade and SCD of RFSoC fitted.

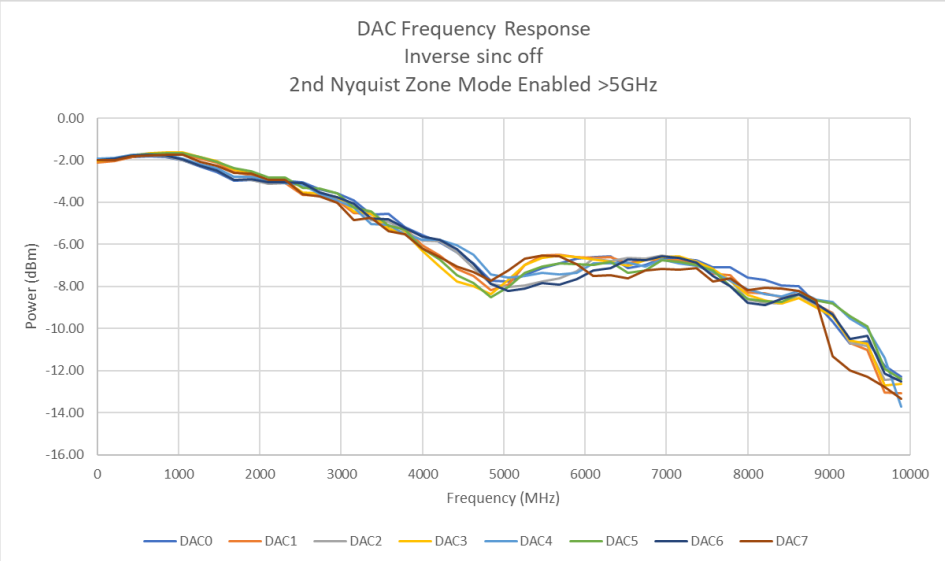

Figure 5 : ADM-XRC-9R1B Gen3 RFSoC DAC Frequency Response

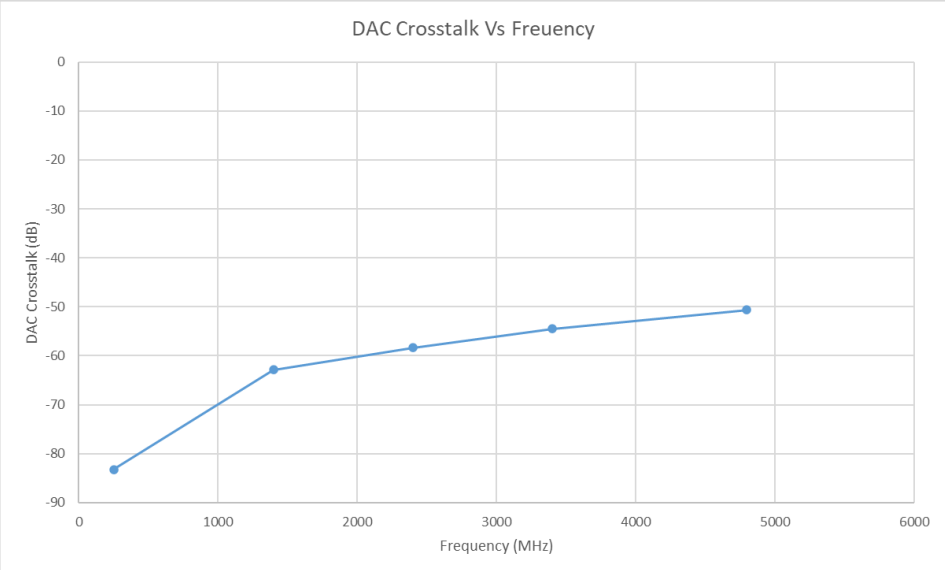

Figure 6 : ADM-XRC-9R1B Gen3 RFSoC DAC Crosstalk

3 Example Design

An FPGA and PS ARM/Linux example design is available, contact support@alpha-data.com for access. It provides an interactive interface or command line interface to control the board features. It can be used to program the RF clocks, drive signals from the DACs, receive data from the ADCs and control the RF converter settings using the Xilinx XRFDC API.

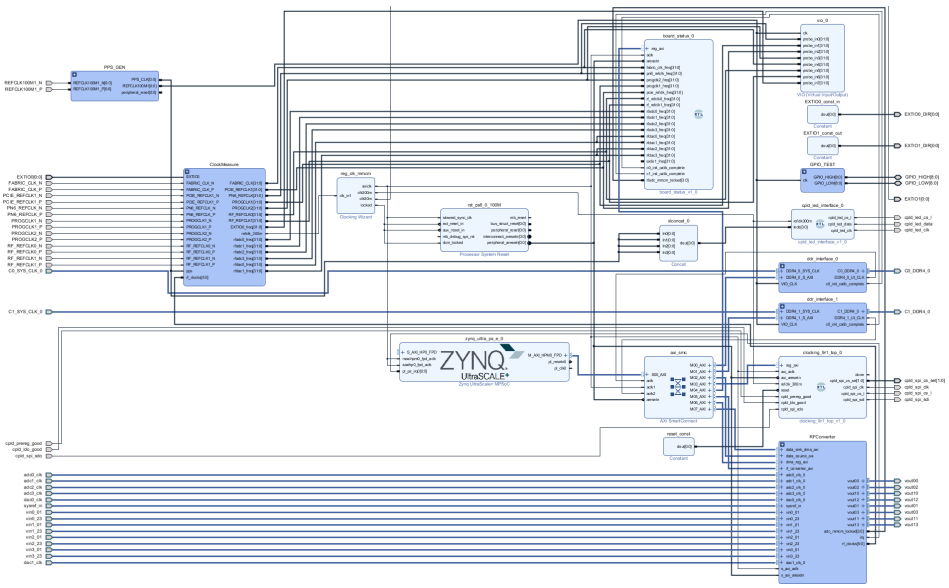

Figure 7 : ADM-XRC-9R1B Vivado Example Design

4 Installation

4.1 Hardware Installation

4.1.1 Handling Instructions

The components on this board can be damaged by electrostatic discharge (ESD). To prevent damage, observe ESD precautions:

- Always wear a wrist-strap when handling the card
- Hold the board by the edges
- Avoid touching any components
- Store in ESD safe bag.

4.1.2 Motherboard / Carrier Requirements

The **ADM-XRC-9R1B** is a single width XMC.3 mezzanine with P6 and P4 connectors. The motherboard/ carrier must comply with the XMC.3 (VITA 42.3) specification for the Primary XMC connector, J5.

The Secondary XMC connector, P6 has a pinout compatible with various XMC to VPX signal maps as defined by VITA 46.9. Please consult the pinouts in this user-guide as-well as those of the carrier manufacturer prior to installation. Assistance can be provided by Alpha Data.

IMPORTANT
Connector P6 on the card is not compatible with the VITA 42.10 (XMC GPIO) Standard. In particular, USB VCC must not be applied on this connector.

The **ADM-XRC-9R1B** is compatible with either 5V or 12V on the "VPWR" power rail.

4.1.3 Cooling Requirements

The power dissipation of the board is highly dependent on the Target FPGA application. A power estimator spreadsheet is available on request from Alpha Data. This should be used in conjunction with Xilinx power estimation tools to determine the exact current requirements for each power rail.

The board is supplied with a passive air cooled or conduction cooled heat-sink according to the order number given at time of purchase. It is the users responsibility to ensure sufficient airflow for air cooled applications and metalwork for conduction cooled applications.

The board features system monitoring that measures the board and FPGA temperature. It also includes a self-protection mechanism that will clear the target FPGA configuration if an over-temperature condition is detected.

See Section 5.9 for further details.

5 Functional Description

5.1 Overview

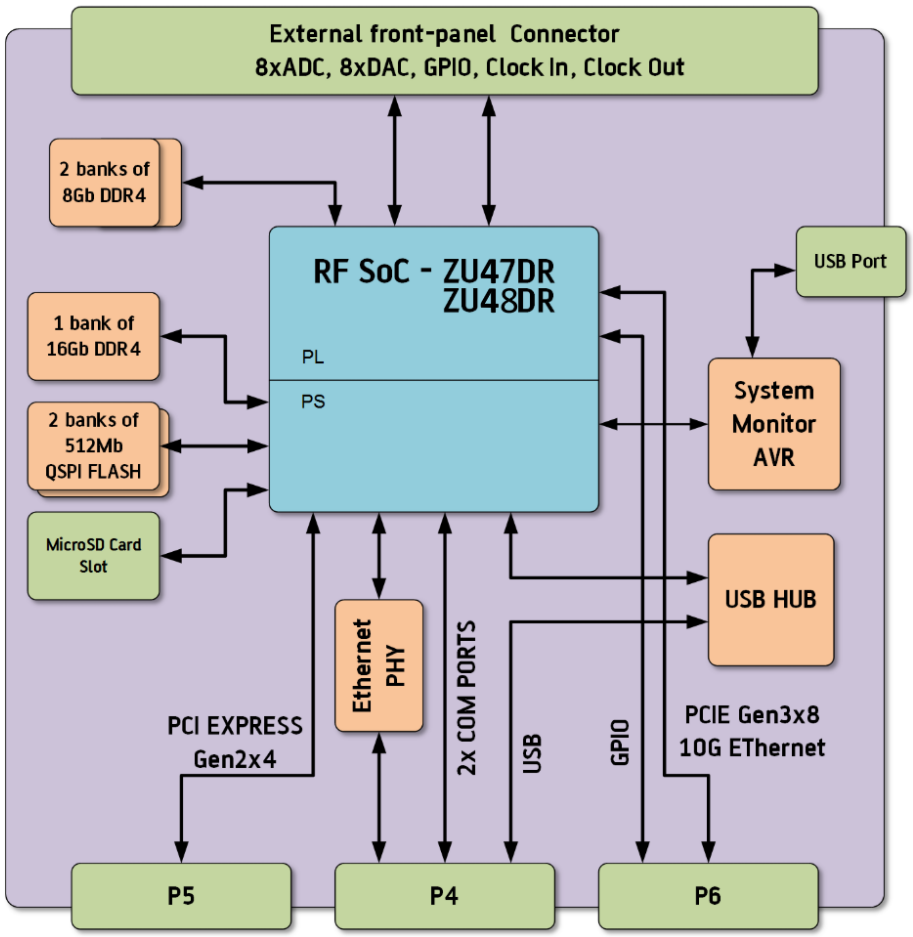

Figure 8 : ADM-XRC-9R1B Block Diagram

5.1.1 Switch Definitions

There is a set of eight DIP switches placed on the rear of the board. Their functions are described in Switch Definitions.

Note:
SW1-5 and SW1-8 are OFF by default. *Factory Configuration* switch must be in the OFF position for normal operation.

Switch Ref.	Function	ON State	Off State
SW1-1	BootMode 0	See Table 17	
SW1-2	BootMode 1	See Table 17	
SW1-3	BootMode 2	See Table 17	
SW1-4	BootMode 3	See Table 17	
SW1-5	*Factory Configuration*	-	Normal Operation
SW1-6	XMC JTAG Enable	XMC JTAG interface is enabled	XMC JTAG interface is disabled
SW1-7	XMC PCIE reset enable	Zynq PS will be reset by the XMC PCIE reset signal	Zynq PS will not be reset by the XMC PCIE reset signal
SW1-8	PS Reset	PS is held in reset	Normal Operation

Table 5 : Switch Definitions

5.1.2 LED Definitions

The position and description of the board status LEDs are shown in LED Locations:

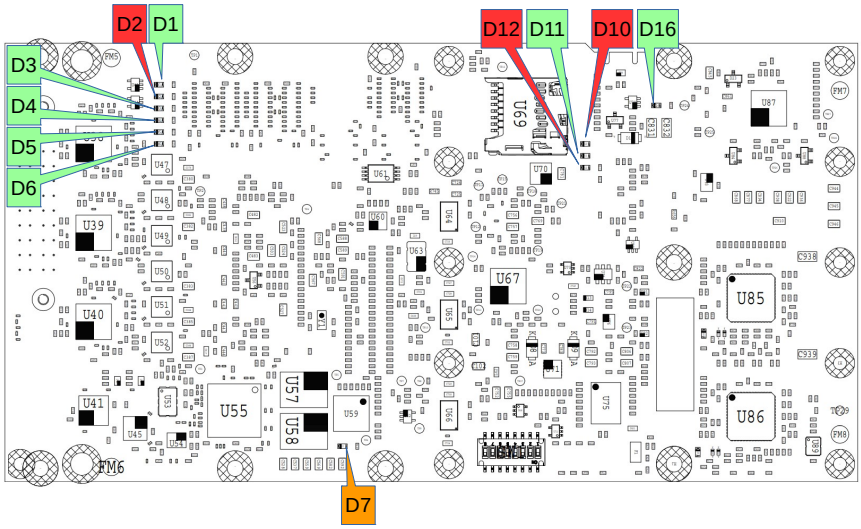

Figure 9 : LED Locations

Comp. Ref.	Function	ON State	Off State
D7(Amber)	MVMRO	Inhibit writes to non-volatile memories	Enable writes to non-volatile memories
D10(Red)	Power Fault	Power supply fault	Normal operation
D11(Green)	Status 0	See Status LED Definitions	
D12(Red)	Status 1	See Status LED Definitions	
D16(Green)	Done	FPGA is configured	FPGA is unconfigured
D2(Red)	PS Error	PS error occurred	No PS error
D1(Green)	PS Status	PS is in secure lockdown state	PS is operating normally
D3(Green)	User Controlled	Pin high	Pin low
D4(Green)	User Controlled	Pin high	Pin low
D5(Green)	User Controlled	Pin high	Pin low
D6(Green)	User Controlled	Pin high	Pin low

Table 6 : LED Definitions

5.1.2.1 User LEDs

The user LEDs are attached to the CPLD and use an SPI interface to control them. The ADM-XRC-9R1B reference design provides VHDL code to control this interface.

5.2 XMC Platform Interface

5.2.1 IPMI I2C

A 2 Kbit I2C EEPROM (type M24C02) is connected to the XMC IPMI. This memory contains board information (type, voltage requirements etc.) as defined in the XMC based specification.

5.2.2 MBIST#

Built-In Self Test. This output signal is connected to FPGA pin K10. It is not driven by default.

5.2.3 MVMRO

XMC Write Prohibit. This signal is an input from the carrier. When asserted (high), all writes to non-volatile memories are inhibited. This is indicated by the Amber LED, D9.

The MVMRO signal has a 100KΩ pull-up resistor fitted by default.

This signal cannot be internally driven or over-ridden. A buffered version of the signal is connected to the PS at pin K19.

5.2.4 MRSTI#

XMC Reset In. This signal is an active low input from the carrier. A this signal connected to the PS at pin G21. This signal can also drive the PS power-on-reset pin depending on SW1-7

A buffered version of MRSTI# is also connected to the FPGA at pin J12.

5.2.5 MRSTO#

XMC Reset Out. This optional output signal is driven from the FPGA pin K12.

5.2.6 MPRESENT#

Module Present. This output signal is connected directly to GND.

5.3 JTAG Interface

5.3.1 On-board Interface

A JTAG boundary scan chain is connected to header U12. This allows the connection of the Xilinx JTAG cable for FPGA debug using the Xilinx ChipScope tools.

Note:
The JTAG adapter connects to header U12 through holes in the PCB, and does not plug directly into the header.

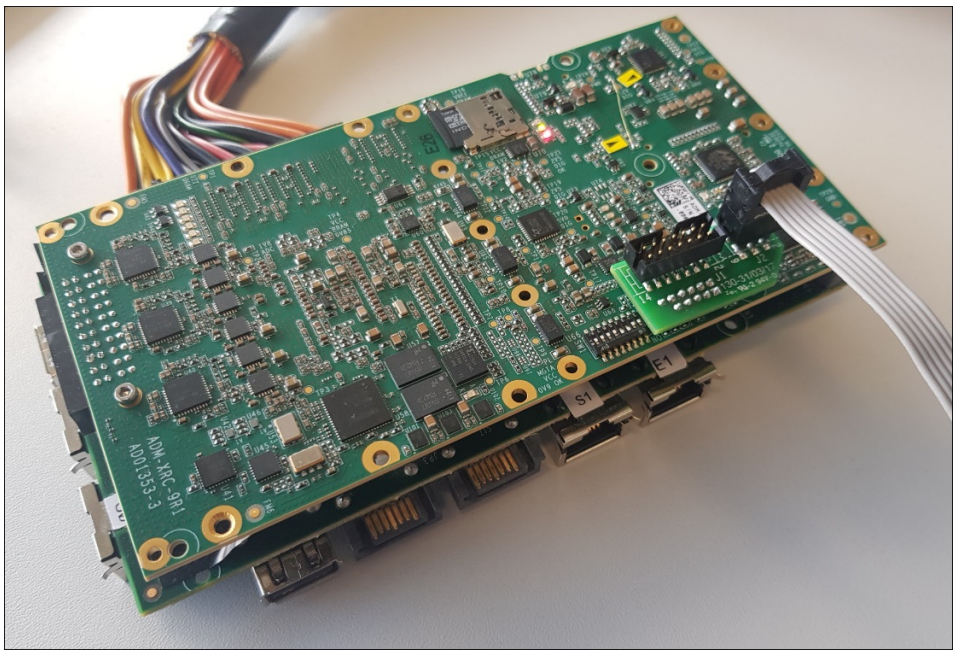

Figure 10 : Connecting the JTAG Adapter

The scan chain is shown in JTAG Boundary Scan Chain:

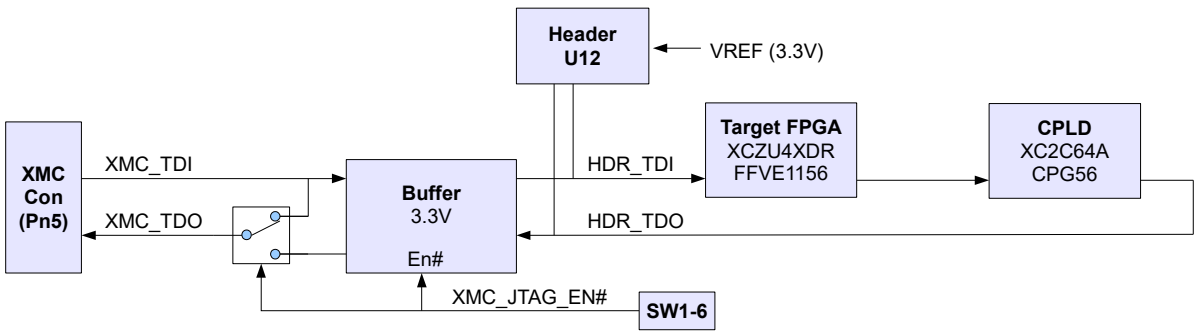

Figure 11 : JTAG Boundary Scan Chain

If the boundary scan chain is connected to the interface at the XMC connector (SW1-6 is ON), Header U12 should not be used.

5.3.2 XMC Interface

The JTAG interface on the XMC connector is normally unused and XMC_TDI connected directly to XMC_TDO.

The interface can be connected to the on-board interface (through level-translators) by switching SW1-6 ON. See Switch Definitions

5.3.3 JTAG Voltages

The on-board JTAG scan chain uses 3.3V. The Vcc supply provided on U12 to the JTAG cable is +3.3V and is protected by a poly fuse rated at 350mA.

The JTAG signals at the XMC interface use 3.3V signals and are connected through level translators to the on-board scan chain.

5.4 Clocks

The **ADM-XRC-9R1B** provides a wide variety of clocking options. The board has a user-programmable clock generator. These clocks can be combined with the FPGA's internal PLLs to suit a wide variety of communication protocols.

The programmable clock source is factory-programmed with a default register map which is automatically configured to the correct values at power-up by the system monitor. The values in the system monitor can be re-programmed and are non-volatile. This means that there is about a 500ms delay between power-up and the clocks being correct and stable. Before this 500ms time, the clocks will be running at default frequencies (REFCLK100M = 250MHz, PROGCLK=156.25MHz, REFCLK300M = 300MHz and FABRIC_CLK = 300MHz)

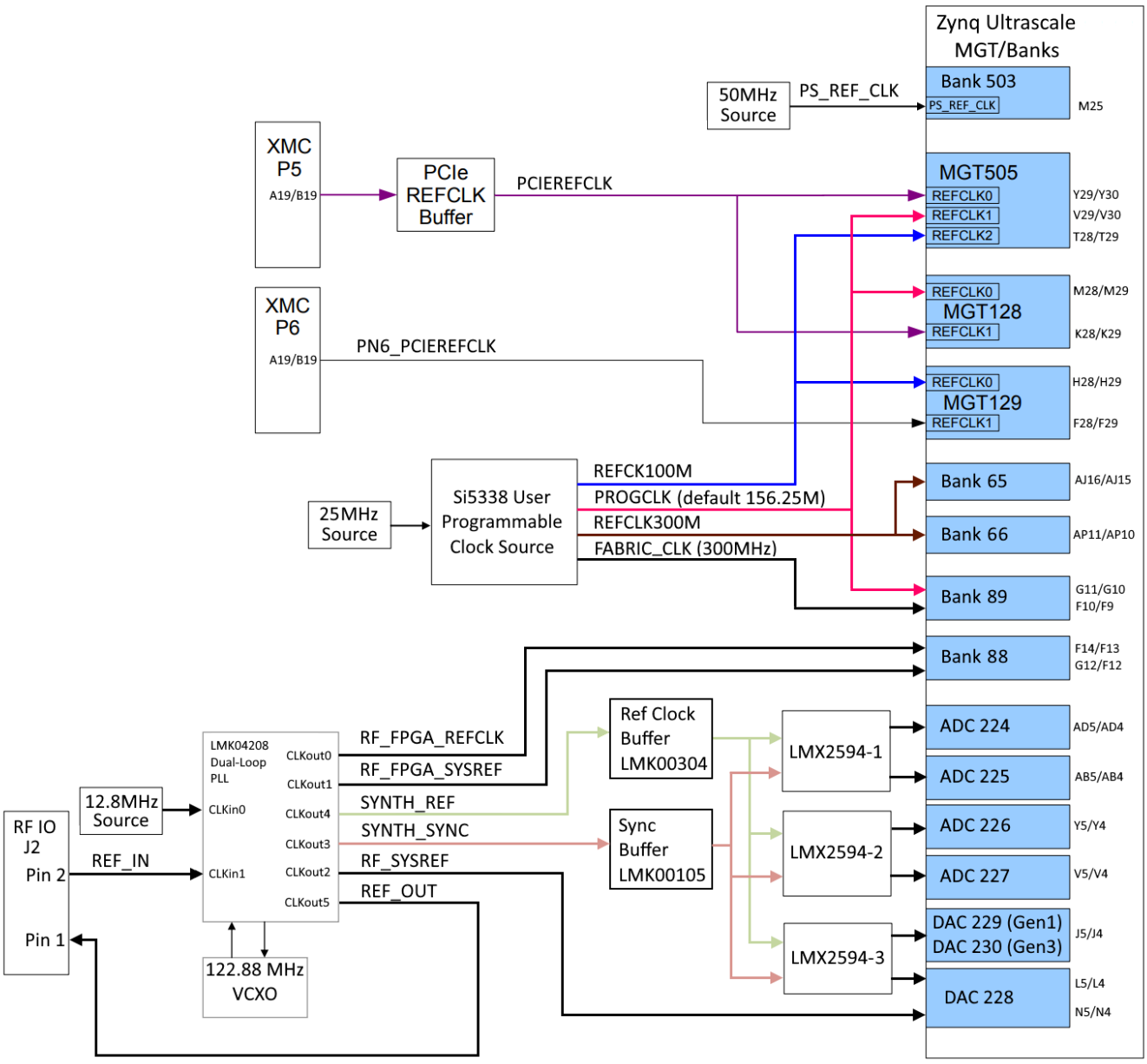

Figure 12 : Full Clock Diagram

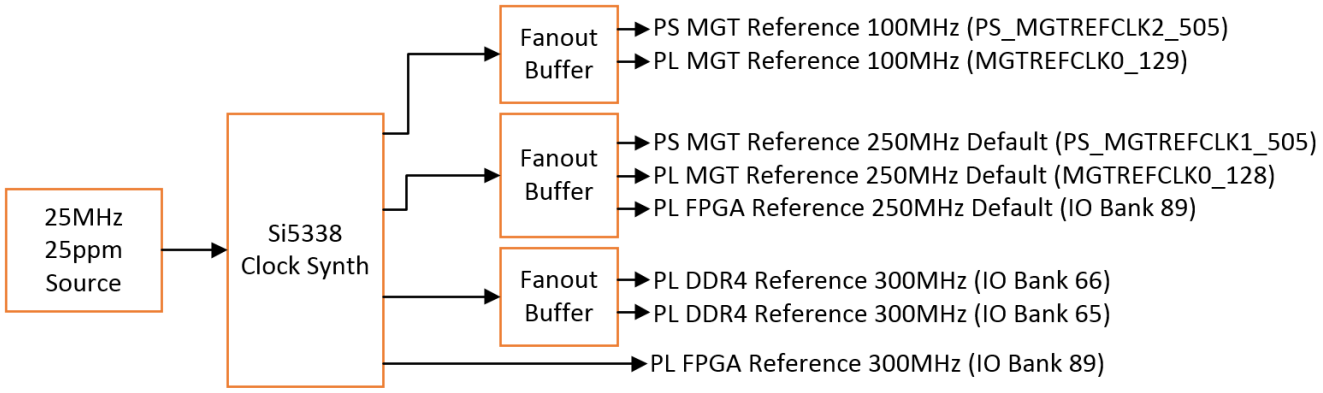

Figure 13 : On-Board Digital System Clocks

5.4.1 300MHz Reference Clocks (REFCLK300M and FABRIC_CLK)

The fixed 300MHz reference clocks REFCLK300M and FABRIC_CLK are differential LVDS signals.

REFCLK300M is distributed through a fanout buffer, and is used as the input clock for both DDR4 SDRAM interfaces.

FABRIC_CLK is used as the reference clock for the IO delay control block (IDELAYCTRL).

Signal	Frequency	Target FPGA Input	IO Standard	"P" pin	"N" pin
REFCLK300M0	300 MHz	IO_L11_T1U_GC_66	LVDS	AP11	AP10
REFCLK300M1	300 MHz	IO_L11_T1U_GC_65	LVDS	AJ16	AJ15
FABRIC_CLK	300 MHz	IO_L7P_HDGC_89	LVDS	F10	F9

Table 7 : REFCLK300M Connections

5.4.2 PCIe Reference Clocks (PCIEREFCLK)

The 100MHz PCI Express reference clock is provided by the carrier card through the Primary XMC connector, P5 at pins A19 and B19. This clock is buffered into two PCIe Express reference clocks that are forwarded to the PS GTR and PL GTY transceivers.

Signal	Frequency	FPGA Input	IO Standard	"P" pin	"N" pin
PCIEREFCLK0	100 MHz	PS_MGTREFCLK0_505	LVDS	Y29	Y30
PCIEREFCLK1	100 MHz	MGTREFCLK1_128	LVDS	K28	K29

Table 8 : PCIEREFCLK Connections

5.4.3 PN6 Reference Clock (PN6_PCIEREFCLK)

The reference clock "PN6_PCIEREFCLK" is a differential clock provided by a carrier card through the Secondary XMC connector P6 at pins A19 and B19. This board connects this pair to an MGT clock input.

Signal	Frequency	FPGA Input	IO Standard	"P" pin	"N" pin
PN6_PCIEREFCLK	100 MHz	MGTREFCLK1_129	LVDS	F28	F29

Table 9 : PN6_PCIEREFCLK Connections

5.4.4 Programmable Clocks (PROGCLK 0-2)

There is one programmable clock source that is forwarded throughout the FPGA. This clock is programmable through the USB system monitor. PROGCLK[2:0] is generated by a dedicated programmable clock generator IC and offer extremely high frequency resolutions (1ppm increments). PROGCLK[2:0] are all buffered copies of the same clock signal.

Signal	Frequency	Target FPGA Input	IO Standard	"P" pin	"N" pin
PROGCLK0	5 - 312.5 MHz	PS_MGTREFCLK1_505	LVDS	V29	V30
PROGCLK1	5 - 312.5 MHz	MGTREFCLK0_128	LVDS	M28	M29
PROGCLK2	5 - 312.5 MHz	IO_L8P_HDGC_89	LVDS	G11	G10

Table 10 : PROGCLK Connections

5.4.5 MGT Reference Clocks

The PS and PL MGTs can be clocked by sources from the P5, P6 or on-board clock sources

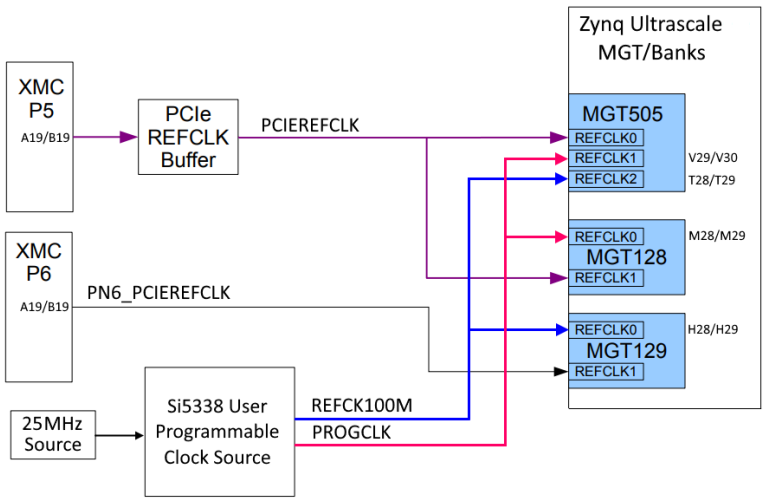

Figure 14 : MGT Clocks

5.4.6 Digital System Oscillators

There are four fixed oscillators on the board for the digital system. The USB and Ethernet reference clocks are used internally by the PHYs.

Signal	Frequency	FPGA pin
PS Ref Clock	50MHz	M25
Si5338 Ref Clock	25MHz	-
USB Ref Clock	24MHz	-
Ethernet Ref Clock	25MHz	-

Table 11 : Reference clocks Connections

5.4.7 RF Sampling Clocks

The RF reference clocks are generated with a dual-loop jitter cleaner PLL. The RF sampling clocks are provided by three LMX2594 RF clock synthesisers.

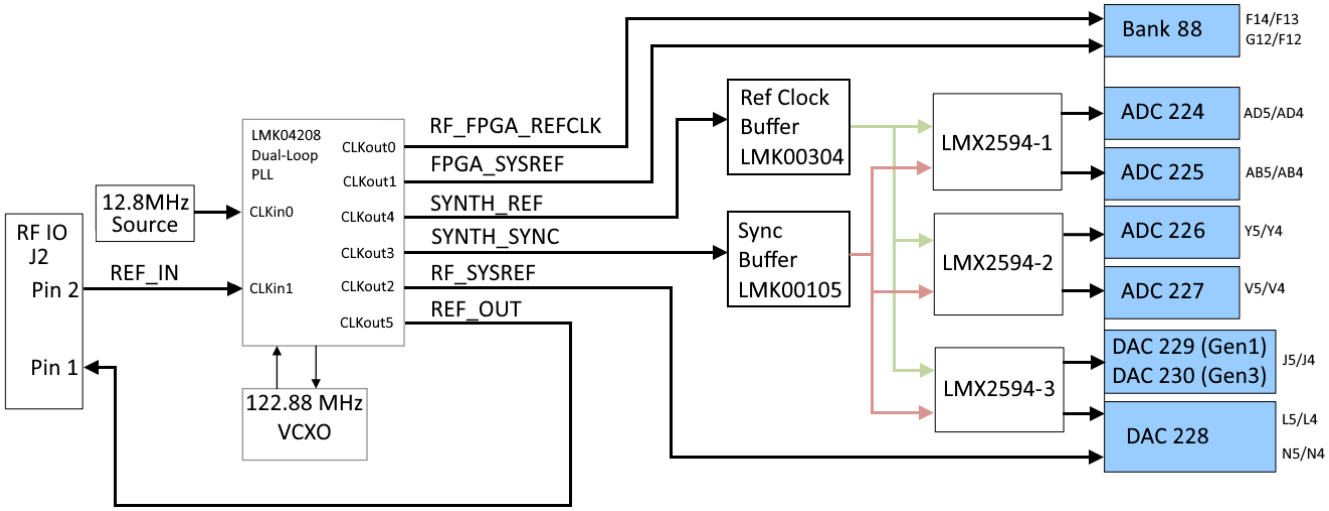

Figure 15 : ADM-XRC-9R1B RF sampling clocks

The external reference clock input amplitude to the LMK04208 is limited by slew rate as well as signal amplitude. It can accept square or sine wave inputs, but with a minimum slew-rate of 0.15V/ns the minimum amplitude with a sine-wave input at 10MHz is quite large. At 10MHz, this would require a ~20dBm signal to meet the slew-rate specs, which would then violate the peak voltage specifications. The LMK04208 clock input voltage range is specified from 0.25-2.4Vpp.

Source	Frequency
External Reference Clock	0.1 - 500MHz
On-Board Reference Clock	12.80MHz
VCXO	122.880MHz

Table 12 : RF Clock Sources

Signal	Frequency	Target FPGA Input	"P" pin	"N" pin
ADC_CLK_224	Variable	ADC_CLK_224	AD5	AD4
ADC_CLK_225	Variable	ADC_CLK_225	AB5	AB4
ADC_CLK_226	Variable	ADC_CLK_226	Y5	Y4
ADC_CLK_227	Variable	ADC_CLK_227	V5	V4
DAC_CLK_228	Variable	DAC_CLK_228	L5	L4
DAC_CLK_229(Gen1) DAC_CLK_230(Gen3)	Variable	DAC_CLK_229 DAC_CLK_230	J5	J4

Table 13 : RF Clock Connections

5.4.7.1 Sysref Clocks

The sysref clocks provide the sysref functionality to synchronize the RF DACs and ADCs. They are provided by the RF clock generators. They are connected to the PL and the RF sampling block.

Signal	Frequency	Target FPGA Input	"P" pin	"N" pin
FPGA Sysref Clock	Variable	IO_L6_HDGC_88	G12	F12
RF Sysref Clock	Variable	SYSREF_228	N5	N4

Table 14 : SysRef Connections

5.4.7.2 RF System FPGA Reference Clock

The RF system FPGA reference clock is a differential clock signal from the RF clock generation circuit, and is connected to an HDGC input on the PL.

Signal	Frequency	Target FPGA Input	"P" pin	"N" pin
RF System FPGA Reference Clock	Variable	IO_L5P_HDGC_88	F14	F13

Table 15 : FPGA Reference Clock Connections

5.4.7.3 RF Clock Programming

The RF reference clocks are programmed from the PL using SPI (LMX2594) or uWire (LMK04208). To minimise FPGA IO pin usage, a CPLD is used to multiplex a single 4-wire IO interface to the FPGA to each of the 4 devices. There are two control bits to select which clock device is active. Both writing and readback are supported for all devices. CPLD Connections shows the required chip select value to access each device.

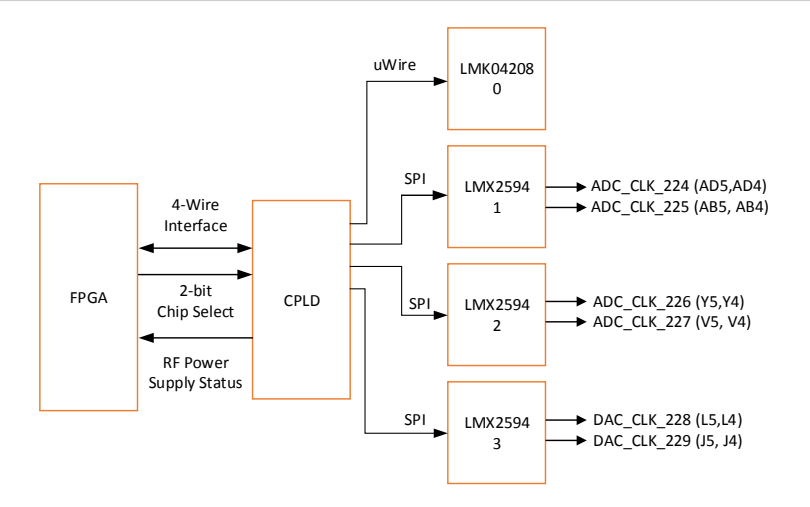

Figure 16 : CPLD Connections

Signal	FPGA Pin	IO Standard	Description
CLK	H13	LVCMOS33	4-Wire interface clock
CS_L	G13	LVCMOS33	4-Wire interface chip select
SDI	E14	LVCMOS33	4-Wire interface data to device (from FPGA)
SDO	D14	LVCMOS33	4-Wire interface data from device (to FPGA)
SPI_SEL[0]	J14	LVCMOS33	Chip select bit 0
SPI_SEL[1]	J13	LVCMOS33	Chip select bit 1
PREREG_PGOOD	H15	LVCMOS33	Power good signal from RF power supplies.
LDO_PGOOD	H14	LVCMOS33	Power good signal from RF power supplies.

Table 16 : FPGA 4-Wire Connections

5.5 Zynq PS Block

5.5.1 Boot Modes

BootMode0 (SW1-1)	BootMode1 (SW1-2)	BootMode2 (SW1-3)	BootMode3 (SW1-4)	Boot Mode
ON	ON	ON	ON	JTAG
ON	OFF	ON	ON	Quad SPI
OFF	OFF	ON	ON	SD Flash
-	-	-	-	Reserved

Table 17 : Boot Mode Selection

5.5.2 Quad SPI Flash Memory

1Gb Flash Memory (2x Micron MT25QU512AB) is used for storing executable code and data for the PS and PL, such as a bootloader, operating system and bitstream. The QSPI memory uses the dual-parallel configuration

The flash memory can only be accessed by the PS.

Utilities for erasing, programming and verification of the flash memory are available in Linux.

5.5.3 MicroSD Flash Memory

A MicroSD card is used for storing executable code and data for the PS and PL, such as a bootloader, operating system and bitstream.

The flash memory can only be accessed by the PS.

5.5.4 PS DDR4 Memory

The **ADM-XRC-9R1B** is fitted with one bank of PS DDR4 SDRAM. The bank is made up of a two 16-bit wide memory devices in parallel to provide a 32-bit datapath capable of running up to 1200MHz (DDR4-2400). 8Gbit devices (Micron MT40A512M16HA-083) are fitted as standard to provide 2GByte of memory.

Full details of the interface, signalling standards and an example design are provided in the ADM-XRC-9R1B example design.

5.5.5 PS MGT Links

There are a total of 4 MGT links connected to the PS Multi-Gigabit Transceivers. See MGT Links for further details

5.5.6 Ethernet Interfaces

The **9R1B** has two 1000BASE-T Ethernet interfaces at rear connector P4 and two 1000BASE-X interfaces at connector P6. The Ethernet PHY will auto-select between either P4 or P6.

Both interfaces have a Marvell 88E1512 PHY, connected to the Zynq via RGMII.

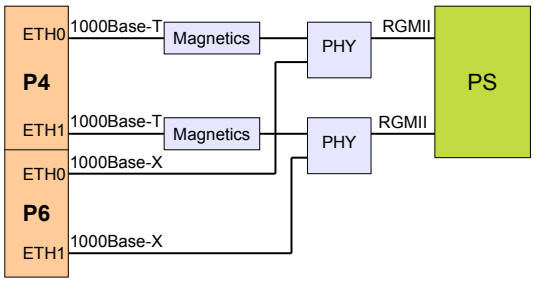

Figure 17 : Ethernet Interfaces

Each interface has three status LEDs. The functions of these are shown in Table 18 below.

LED	Colour	Function
0	Green	On = Link up, Flashing = RX activity
1	Green	unused
2	Amber	On = Link up, Flashing = TX activity

Table 18 : Ethernet Status LEDs

5.5.7 Serial COM Ports

There are two serial COM ports connected to PMC connector P4, as shown in Figure Serial COM Ports. The default speed of the COM ports is 115.2k.

COM2 uses RS-232 by default but may be configured for RS-485 operation. Please contact Alpha Data for further details of the RS-485 mode.

COM0 and COM2 are both connected to PS UART1, and are therefore mutually exclusive due to the PS only having two UART interfaces.

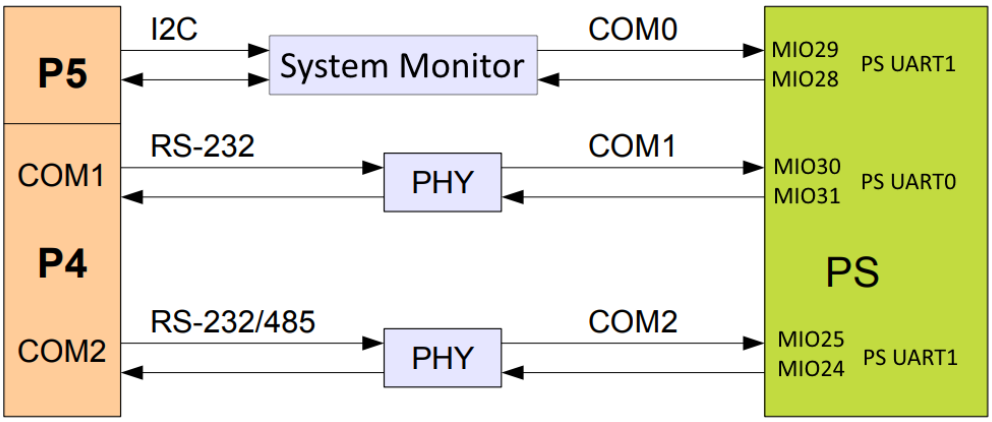

Figure 18 : Serial COM Ports

5.5.8 USB Interfaces

The **ADM-XRC-9R1B** has two external USB interfaces connected to rear connector P4.

The Zynq PS is configured as the USB host to the external interfaces.

The on-board system monitor is accessible from the micro-USB connector

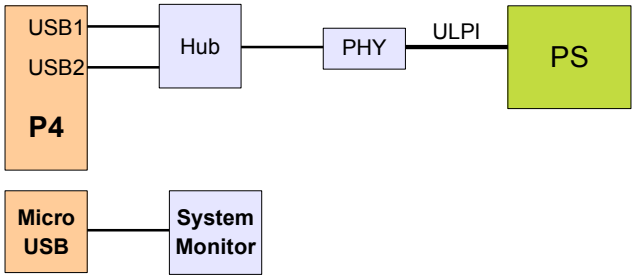

Figure 19 : USB Interfaces

5.6 PL Interfaces

5.6.1 I/O Bank Voltages

The Target FPGA IO is arranged in banks, each with their own supply pins. The bank numbers, their voltage and function are shown in Target FPGA IO Banks. Full details of the IOSTANDARD required for each signal are given in the ADM-XRC-9R1B example design.

IO Banks	Voltage	Purpose
503	3.3V	Configuration, JTAG, Boot Mode Select
89	3.3V	PN6 GPIO
65, 66	1.2V	DRAM Banks 0-1

Table 19 : Target FPGA IO Banks

5.6.2 MGT Links

There are a total of 8 Multi-Gigabit Transceiver (MGT) links connected to the Target FPGA, and 4 links to the PS:

Links	Width	Connection
P6(7:0)	8	Direct link to XMC P6 lanes (7:0)
P5(7:0)	4	Direct link to XMC P4 lanes (3:0)

Table 20 : Target MGT Links

The connections of these links are shown in MGT Links:

For MGT Clocking see MGT Clocks:

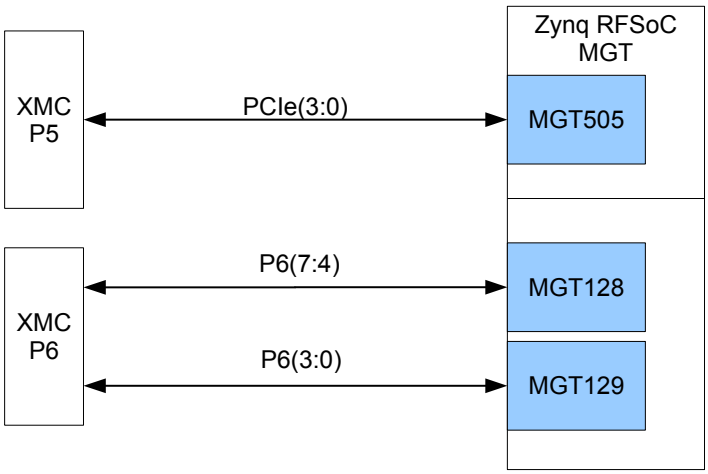

Figure 20 : MGT Links

5.6.3 Memory Interfaces

The **ADM-XRC-9R1B** has two independent banks of DDR4 SDRAM. Each bank consists of one 8-bit wide memory device capable of running at up to 1200MHz (DDR-2400). 8Gbit devices (Micron MT40A1G8PM-083E) are fitted as standard.

The memory banks are arranged for compatibility with the Xilinx Memory Interface Generator (MIG). PL DRAM Banks shows the component references and FPGA banks used. Full details of the interface, signalling standards and an example design are provided in the ADM-XRC-9R1B example design.

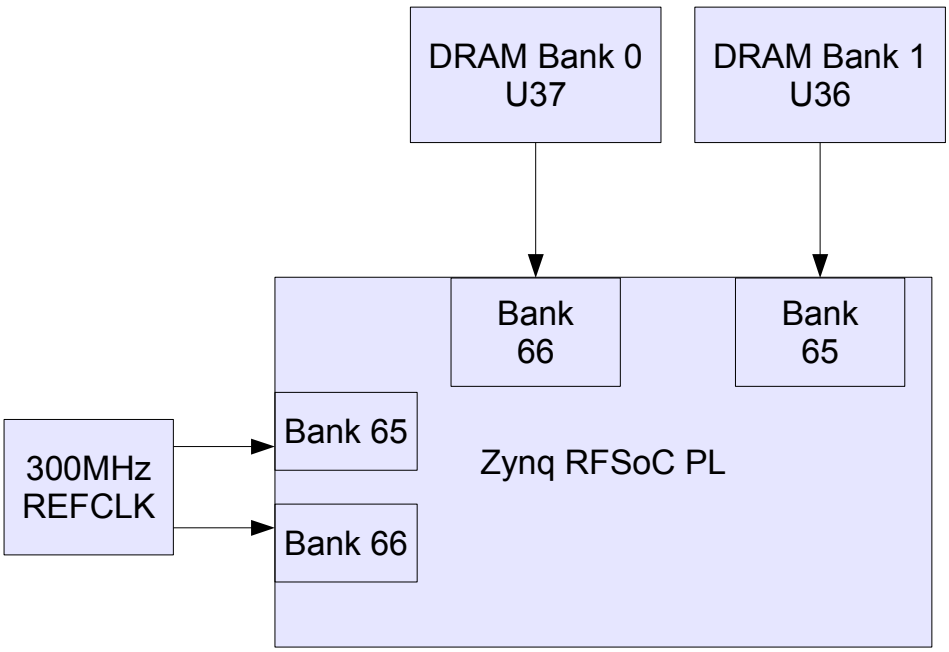

Figure 21 : PL DRAM Banks

5.6.4 GPIO

There are 19 GPIO pins from the FPGA, which are compatible with 3.3V signalling such as TTL and CMOS. These GPIO pins are passed through a Texas Instruments TXS0108E level translator, capable of open-drain and push-pull level translation. The level translator is auto direction sensing. The level translator has a propagation delay of 5.7ns max and a channel-to-channel skew (within a package) of 1ns. Therefore, it is only suitable for rates up to ~50Mb/s.

The level translators have built-in pull-up resistors with a value of 4kΩ.

The GPIO pin mapping is shown in Pn6 GPIO Pin Map.

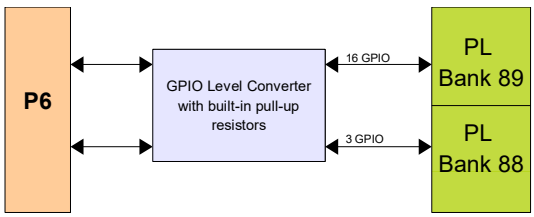

Figure 22 : GPIO Block Diagram

5.7 RF Interfaces

5.7.1 Front-Panel I/O

The front panel interface consists of a pair of 8-way high-speed locking connectors J3 and J4, and an IO mezzanine board with four SSMC connectors. These support 8 DAC signals, 8 ADC signals, two GPIO, an input RF reference clock, and an output RF reference clock. The connector part number is Rosenberger 23C25H-40ML5.

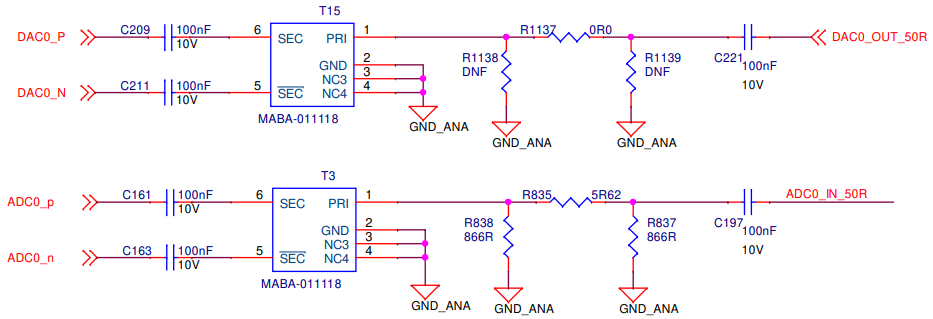

Figure 23 : Front Panel RF IO Transformers

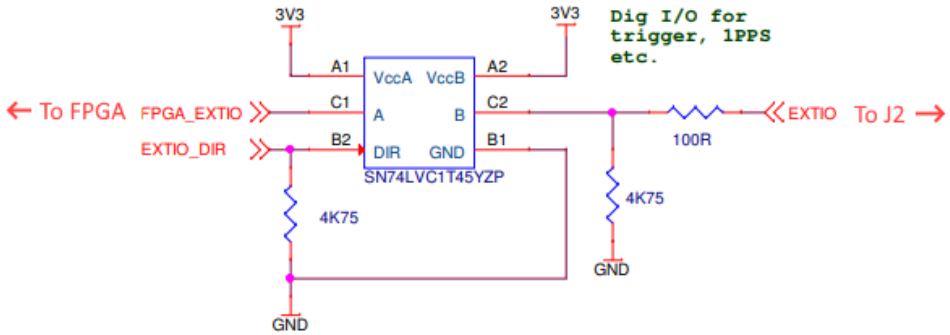

Figure 24 : Front Panel EXTIO Buffers

The EXTIO signals are buffered through level translators, with direction controlled by FPGA. The direction pin should be low for input, high for output. There is a pull-down resistor to ensure the EXTIO signals are input by default. These level translators will provide some ESD/over voltage protection to the FPGA inputs, and have a maximum data rate of 210Mbps.

Boards are fitted with MABA-011118 10MHz-10GHz transformers to convert from 50 Ohm single-ended to 100 Ohms differential.

The DAC operates in variable output power mode (with 3.0V DAC_AVTT).

The ADC voltages in the table below are the single ended voltages at the RF connector. The DAC voltages are the voltages driving a 50 Ohm impedance.

Signal	Impedance (Ohms)	Pin number	FPGA Pin
ADC IO			ERROR
ADC0	50	J3-8	AK2/AK1
ADC1	50	J3-7	AH2/AH1
ADC2	50	J3-6	AF2/AF1
ADC3	50	J3-5	AD2/AD1
ADC4	50	J3-4	AB2/AB1
ADC5	50	J3-3	Y2/Y1
ADC6	50	J3-2	V2/V1
ADC7	50	J3-1	T2/T1
DAC IO			ERROR
DAC0	50	J4-8	N2/N1
DAC1	50	J4-7	L2/L1
DAC2	50	J4-6	J2/J1
DAC3	50	J4-5	G2/G1
DAC4	50	J4-4	E2/E1
DAC5	50	J4-3	C2/C1
DAC6	50	J4-2	B4/A4
DAC7	50	J4-1	B6/A6
Digital IO			ERROR
REF IN	50	J4	-
REF OUT	50	J5	-
EXTIO0	-	J3	A14
EXTIO0_DIR	-	-	A13
EXTIO1	-	J2	B12
EXTIO1_DIR	-	-	A12

Table 21 : Front panel I/O signals

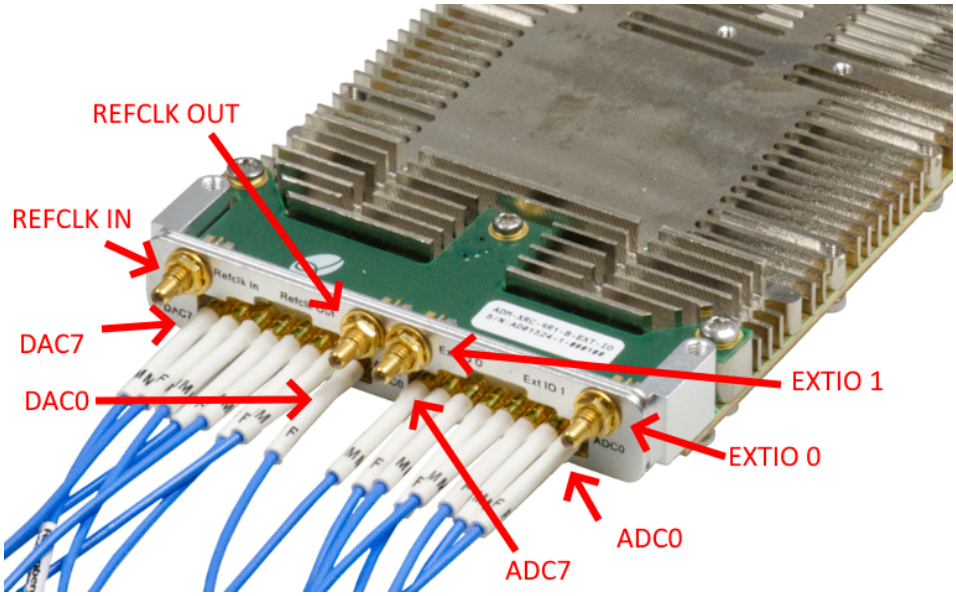

Figure 25 : RF Connector Pinout

5.8 Configuration

5.8.1 Power-Up Sequence

At power-up, the PS will load the first-stage bootloader from the memory interface selected by the Boot Mode select switches.

The first stage bootloader is responsible for configuring the FPGA and PS attached interfaces.

> **Note:**
> If an over-temperature alert is detected from the System Monitor, the target **will be cleared** by pulsing its PROG signal. See Automatic Temperature Monitoring.

5.9 System Monitoring

The **ADM-XRC-9R1B** has the ability to monitor temperature and voltage to maintain a check on the operation of the board. The monitoring is implemented using the Atmel AVR microcontroller.

Control algorithms within the microcontroller automatically check line voltages and on board temperatures and shares the information with the PS.

The following voltage rails and temperatures are monitored:

Monitor	*Purpose*
VPWR	Board Input Supply (either 5.0V or 12.0V)
12.0V	Board Input Supply
5.0V	Internally generated 5V supply
3.3V	Board Input Supply
3.3V	Internally generated 3.3V supply
2.5V	Digital clocks and DDR4
1.8V	Flash Memory, FPGA IO Voltage (VCCO)
0.85V	FPGA Core Supply (VccINT)
1.8V	Transceiver Power (AVCC_AUX)
1.2V	DDR4 SDRAM, memory I/O
0.85V	Block RAM and SD-FEC supply (VccBRAM)
1.2V	Transceiver Power (AVTT)
0.9V	Transceiver Power (AVCC)
0.85V	PS VCC power (PSVccINT)
Temp0	Microcontroller on-die temperature
Temp1	Board temperature sensor on-die temperature
Temp2	FPGA on-die temperature

Table 22 : Voltage and Temperature Monitors

5.9.1 Automatic Temperature Monitoring

At power-up, the control logic sets the temperature limits and resets the LM87's over-temperature interrupt.

The temperature limits are shown in Table Temperature Limits:

	FPGA		Board	
	Min	Max	Min	Max
Commercial	0 degC	+85 degC	0 degC	+85 degC
Extended	0 degC	+100 degC	0 degC	+100 degC
Industrial	-40 degC	+100 degC	-40 degC	+100 degC

Table 23 : Temperature Limits

Note:
If any temperature limit is exceeded, the FPGA is automatically cleared. This is indicated by the Green LED (Target Configured) switching off and the two status LEDs showing a temperature fault indication.

The purpose of this mechanism is to protect the card from damage due to over-temperature. It is possible that it will cause the user application and, possibly, the host computer to "hang".

5.9.2 Microcontroller Status LEDs

LEDs D12 (Red) and D11 (Green) indicate the microcontroller status.

LEDs	*Status*
Green	Running and no alarms
Green + Red	Standby (Powered off)
Flashing Green + Flashing Red (together)	Attention - critical alarm active
Flashing Green + Flashing Red (alternating)	Service Mode
Flashing Green + Red	Attention - alarm active
Red	Missing application firmware or invalid firmware
Flashing Red	FPGA configuration cleared to protect board

Table 24 : Status LED Definitions

5.9.3 System Monitor Interfaces

There are two ways to communicate with the System Monitor to retrieve board status information on the ADM-XRC-9R1B. One is through the Micro USB connector (shown in USB Interfaces), the other is using one of the PS UART interfaces (shown in Serial COM Ports). These communication interfaces are intended to be used with Alpha-Data utility called avr2util. Avr2util is provided with the 9R1B PetaLinux BSP, and can be run from the ADM-XRC-9R1B once booted.

To see available options, run:

```
avr2util -?
```

To display sensor values (use -psuart for the PS UART interface, or -usbcom for the MicroUSB interface):

```
avr2util -psuart /dev/ttyPS1,170000 display-sensors
```

To set the user-programmable clock (e.g. PROGCLK at index 1) to 156.25MHz:

```
avr2util -psuart /dev/ttyPS1,170000 setclknv 1 156250000
```

Clock	Index
PCIEREFCLK	0
PROGCLK	1
REFCLK300M	2
FABRIC_CLK	3

Table 25 : avr2util clock indexes

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Appendix A: Rear Connector Pinouts

Appendix A.1: Primary XMC Connector, P5

	A	B	C	D	E	F
1:	PET_P0	PET_N0	3V3	PET_P1	PET_N1	VPWR
2:	GND	GND	-	GND	GND	MRSTI_L
3:	PET_P2	PET_N2	3V3	PET_P3	PET_N3	VPWR
4:	GND	GND	TCK	GND	GND	MRSTO_L*
5:	-	-	3V3	-	-	VPWR
6:	GND	GND	TMS	GND	GND	12V0
7:	-	-	3V3	-	-	VPWR
8:	GND	GND	TDI	GND	GND	M12V0
9:	-	-	-	-	-	VPWR
10:	GND	GND	TDO	GND	GND	GA0
11:	PER_P0	PER_N0	MBIST_L*	PER_P1	PER_N1	VPWR
12:	GND	GND	GA1	GND	GND	MPRESENT_L
13:	PER_P2	PER_N2	3V3_AUX	PER_P3	PER_N3	VPWR
14:	GND	GND	GA2	GND	GND	I2C_SDA
15:	-	-	-	-	-	VPWR
16:	GND	GND	MVMRO	GND	GND	MSCL
17:	-	-	-	-	-	-
18:	GND	GND	-	GND	GND	-
19:	REFCLK0_P	REFCLK0_N	-	WAKE_L	ROOT0_L	-

Table 26 : Pn5 Interface

*FPGA pins MRSTO_L and MBIST_L are disconnected by default (with MRSTO_L pulled high with a pull-up resistor). Please contact Alpha Data for further details if this is required.

Appendix A.2: Secondary XMC Connector, P6

.	A	B	C	D	E	F
1:	PN6_TX_P0	PN6_TX_N0	P6_USB1_DP	PN6_TX_P1	PN6_TX_N1	P6_COM1_RXD
2:	GND	GND	P6_USB1_DM	GND	GND	P6_COM1_TXD
3:	PN6_TX_P2	PN6_TX_N2	P6_USB1_VBUS	PN6_TX_P3	PN6_TX_N3	P6_COM2_TXP
4:	GND	GND	P6_USB2_DP	GND	GND	P6_COM2_TXN
5:	PN6_TX_P4	PN6_TX_N4	P6_USB2_DM	PN6_TX_P5	PN6_TX_N5	P6_COM2_RXP
6:	GND	GND	P6_USB2_VBUS	GND	GND	P6_COM2_RXN
7:	PN6_TX_P6	PN6_TX_N6	GP18	PN6_TX_P7	PN6_TX_N7	GND
8:	GND	GND	GP17	GND	GND	ETH1_TX_P
9:	-	-	GP16	ETH0_TX_P	ETH0_TX_N	ETH1_TX_N
10:	GND	GND	GP15	GND	GND	GND
11:	PN6_RX_P0	PN6_RX_N0	GP14	PN6_RX_P1	PN6_RX_N1	ETH1_RX_P
12:	GND	GND	GP13	GND	GND	ETH1_RX_N
13:	PN6_RX_P2	PN6_RX_N2	GP12	PN6_RX_P3	PN6_RX_N3	GND
14:	GND	GND	GP10	GND	GND	GP11
15:	PN6_RX_P4	PN6_RX_N4	GP8	PN6_RX_P5	PN6_RX_N5	GP9
16:	GND	GND	GP6	GND	GND	GP7
17:	PN6_RX_P6	PN6_RX_N6	GP4	PN6_RX_P7	PN6_RX_N7	GP5
18:	GND	GND	GP2	GND	GND	GP3
19:	REFCLK0_P	REFCLK0_N	GP0	ETH0_RX_P	ETH0_RX_N	GP1

Table 27 : Pn6 Interface

Appendix A.2.1: Pn6 GPIO Pin Map

Signal	P6 Pin	FPGA Pin	FPGA Bank
GP0	C19	B13	88
GP1	F19	C13	88
GP2/MBIST#*	C18	K10	89
GP3	F18	A10	89
GP4	C17	H9	89
GP5	F17	C10	89
GP6	C16	H10	89
GP7	F16	E9	89
GP8	C15	E10	89
GP9/MRSTO#*	F15	K12	89
GP10	C14	C11	89
GP11	F14	C14	88
GP12	C13	D11	89
GP13	C12	E11	89
GP14	C11	A9	89
GP15	C10	B11	89
GP16	C9	B10	89
GP17	C8	C9	89
GP18	C7	D9	89

Table 28 : Pn6 GPIO Pin Map

*FPGA pins K10 and K12 can optionally drive MRSTO# and MBIST# on the XMC P5 connector. Please contact Alpha Data for further details if this is required.

Appendix A.3: PMC Connector P4

Signal	P4 Pin	P4 Pin	Signal
P4_ETH0_MDI_0_P	1	2	P4_ETH0_MDI_2_P
P4_ETH0_MDI_0_N	3	4	P4_ETH0_MDI_2_N
GND	5	6	GND
P4_ETH0_MDI_1_P	7	8	P4_ETH0_MDI_3_P
P4_ETH0_MDI_1_N	9	10	P4_ETH0_MDI_3_N
GND	11	12	GND
P4_ETH1_MDI_0_P	13	14	P4_ETH1_MDI_2_P
P4_ETH1_MDI_0_N	15	16	P4_ETH1_MDI_2_N
GND	17	18	GND
P4_ETH1_MDI_1_P	19	20	P4_ETH1_MDI_3_P
P4_ETH1_MDI_1_N	21	22	P4_ETH1_MDI_3_N
GND	23	24	GND
P4_USB1_DM	25	26	P4_USB2_DM
P4_USB1_DP	27	28	P4_USB2_DP
P4_USB1_VBUS	29	30	P4_USB2_VBUS
-	31	32	-
-	33	34	-
-	35	36	-
-	37	38	-
-	39	40	-
-	41	42	P4_COM1_RXD
P4_COM1_TXD	43	44	-
P4_COM2_TXN	45	46	P4_COM2_RXN
P4_COM2_TXP	47	48	P4_COM2_RXP
-	49	50	-
-	51	52	-
-	53	54	-
-	55	56	-
-	57	58	-
-	59	60	-
-	61	62	-
-	63	64	-

Table 29 : Pn4 Interface

Revision History

Date	Revision	Nature of Change	Section(s)
27th September 2024	1.0	First Release.	
14th October 2024	1.1	Added info about GPIO pull-ups, added JTAG adapter picture	Section 5.6.4, Section 5.3

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